ABSTRACT

A system (10) for interconnecting two modules (100, 100') to the CPU ~~CUP~~ chip, includes two opposite connectors (12, 14) in a head-to-head arrangement. The traces (200) each of which connects the two corresponding contacts 28/30 and 30'/28' each being located in the same position of the corresponding connector (12, 14), are generally arranged in a parallel relationship. One (12) of the connectors (12, 14) is substantially a standard one which meets the requirements defined in the general specification. The other (14) of the connectors (12, 14) is generally, but not exactly, of a mirror image with regard to the first one (12), wherein the positions of the two-row contacts (28'/30') with regard to the housing (16') along the lengthwise direction of the second connector (14) are arranged in an opposite relationship with regard to those in the first connector (12). When used, a standard module (100) can be inserted into the first connector (12) in a common way with its upside surface (106) facing up, or can be inserted into the second connector (14) in an opposite way with its back surface (108) facing up, whereby the pads (P1-P144) printed on both surfaces (106, 108) of the module (100,, 100') can be respectively properly electrically connected to the corresponding traces (200) regardless of which connector (12, 14) it is inserted into.